ALD deposited thin HfO_2 films: electrical and structural characterization.

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The further dimensional shrinking of MOS devices is necessary in order to follow the continuous requirement of faster devices for technological applications. Towards this goal, new substrates, such as s-Si, Ge and III-V semiconductors, with higher carrier mobility than Si are studied [1,2].On the other hand, in order to replace SiO_2, "new" high-k materials such as ZrO_2, Al_2O_3, HfO_2 are also studied [3,4].
ALD is one of the most promising deposition technique in microelectronics because it gives the opportunity to deposit ultra thin films at relatively low temperatures with absolute control of the thickness. HfO_2 is a promising gate dielectric material mainly due to the high dielectric value (20-25). In this study we deposit HfO_2 dielectric films, in pre-cleaned p-Ge substrates via ALD technique in three different deposition temperatures. X-ray Photoelectron Spectroscopy (XPS) analysis revealed that stoichiometrical HfO_2 was deposited in all three deposition temperatures.
AFM analysis reveals that HfO_2 films are uniform, cohesive with very low roughness. In order to electrically characterize these structures, Pt/HfO_2/p-Ge structures were constructed through photolithography and lift off methods. The electrical response as well as the Density of Interfacial traps (D_{it})of the structures were tested/evaluated through C-V, C-f and G-V measurements. A passivation layer of plasma grown GeO_2 (2nm) was developed in between the gate dielectric and the Ge substrate. The structures were also characterized by C-V, C-f and G-V measurements.

References

[1] K.C. Saraswat et al. Microelectron. Eng., **80**, 15 (2005).
[2] M.A. Botzakaki et al., Microelectron. Eng. **112**, 208 (2013).
[3] J.M. Rafi et al.J. Electrochem. Soc. **158** (5) G108 (2011).
[4] Z. Tan et al. ECS Solid State Lett. **2** (8) P61-P62 (2013).

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